Simulation and Analysis of P/G Noise in TSV based 3D MPSoC

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***Abstract*—3D multi-processor system-on-chip (3D MPSoC) can integrate more PUs together with shorter interconnection using vertical interconnection. It's very important to analyze the power ground (P/G) noise induced by power gating in low power 2D MPSoC. Actually, 3D MPSoC will be more sensitive to P/G noise due to the vertical interconnection between different *PU*s. So the P/G noise induced by power gating needs more attention in low power 3D MPSoC design. In this paper, we firstly build a TSV-based 3D MPSoC P/G noise simulation platform. Then with the platform, several experiments are conducted to explore the P/G noise induced by power gating. At last, we investigate the proper distribution for P/G TSVs and the P/G noise propagation in 3D MPSoC.**

I. INTRODUCTION

In recent years，with continued technology scaling, interconnect has become a significant issue in the design of integrated circuits and emerged as the main source of power consumption and circuit delay. The traditional planar Chip Multi-Processor (CMP) architectures are facing some difficult problems due to on-chip interconnects are not scaling with technology [1]. Three-dimensional (3D) integration has been regarded as a promising solution to mitigate the interconnect-related problems [2] [3] [4] [5]. Different methods are proposed to connect the tiers in 3D design, including wire bonded, micro-bump, contactless (inductive and capacitive), and through silicon via (TSV) [2]. TSV is thought to be the most promising one.

MPSoCs use multiple or even many processing units (*PU*s) in order to deliver additional system performance within their power budget. Strict low power requirements have led to the adoption of some techniques such as dynamic voltage and frequency scaling, clock gating and power gating [6][7], among which power gating is a mature solution to eliminate the ever-increasing leakage power consumption. However, when a new task is assigned to a power-off *PU* or a *PU* finishes a task, the powering on/off will cause large noise in the power delivery network and then propagate to the *PU*s around the powering-on/off *PU*. Especially in 3D MPSoC, the power supply noise induced by power gating will propagate to other *PU*s more easily due to shorter interconnect compared with 2D MPSoC. As a result, it's quite necessary to model and analyze the P/G noise in 3D MPSoC to fulfill the low power and high reliability requirements. To the best of our knowledge, there are few studies addressing such noise issues in 3D MPSoC. This paper will focus on P/G noise induced by power gating. We use simulation based approaches to search for the proper distribution of P/G TSVs and analyze the P/G noise propagation performance in 3D MPSoC, which is useful for 3D MPSoC designers when considering power gating techniques.

The rest of this paper is organized as follows. Section II gives an overview of previous work. P/G noise analysis platform including the P/G network model of MPSoC and TSV model is provided in section III. Section IV shows the experimental results and related analysis. Section V concludes the paper and proposes the future work.

II. RELATED WORK

In the last few years, 3D ICs have attracted considerable attention from industry and academia as a potential way to solve the interconnect bottleneck problem facing 2D ICs. The current 3D IC research is mainly about how to take advantage of the performance, power, smaller form-factor and heterogeneous integration benefits brought by 3D integration [8]. Different 3D stacking technologies considering performance improvement and implementation cost are proposed in [9] [10] [11]. The bonding between adjacent tiers can be characterized by the orientation of each tier, including Face-to-Back (F2B), Face-to-Face (F2F) and Back-to-Back (B2B) [3]. TSVs and micro-bumps are key technologies to realize 3D chip stacks for high-performance applications. Vertical interconnects implemented as TSVs bring the highest interconnect bandwidth in 3D ICs, compared to wire bonding, peripheral vertical interconnects and solder ball arrays. So this paper focuses on TSV based 3D MPSoC. Some TSV models and related parameters are discussed in [12] [13] [14] [22].

Although 3D IC integration can improve signal interconnection, it also brings new challenges, especially in power delivery and cooling ("thermal interconnects"). Several key challenges and promising technologies to address power delivery are discussed in [14]. Large amount of current needs to be delivered through limited footprint area when multiple high-power microprocessors are stacked together and flip-chip technology for 3D chip stacking is

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used, which may lead to some noise issues if some functional blocks switch simultaneously. Hence, power distribution networks in 3D systems need to be accurately modeled and carefully designed [14]. An analytical physical model of P/G network is derived to incorporate the impact of 3D-integration on power supply noise in [15]. Simulation results show the model has less than 4% error compared to SPICE simulations. [15] also gives some design guidelines and opportunities for reducing power supply noise, such as inserting "decap" die and TSVs. As concluded in [15], 3D IC can not benefit by solely increasing the number of TSVs of each tier. However, the TSV model is very simple and they do not consider the powering on/off even in 3D MPSoC.

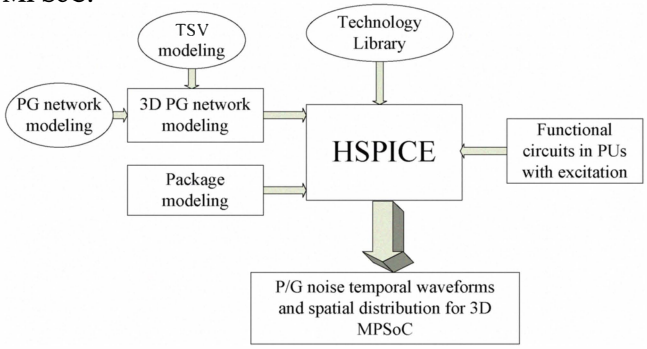

Fig. 1 Power Gating induced P/G noise analysis platform for 3D MPSoC

III. P/G Noise Simulation and Analysis Platform

In this section, our power gating induced P/G noise analysis platform for the TSV-based 3D MPSoC is introduced. The framework of the platform is shown in Fig. 1. There are three key components in the platform: 1) 3D P/G network modeling and package modeling of 3D MPSoC. 2) MPSoC specification, such as *PU* number, layout, behavior and so on; 3) Technology parameters, such as technology node related physical parameters, P/G TSV related parameters and etc. We can get the P/G noise induced by powering on/off *PU*s in different position and with different number of tiers. We can change the distribution of P/G TSVs in each tier to search for proper location of P/G TSVs.

Firstly we will give a overview of our platform. Then related models, including P/G network model, package model and vertical interconnection model, will be described in detail.

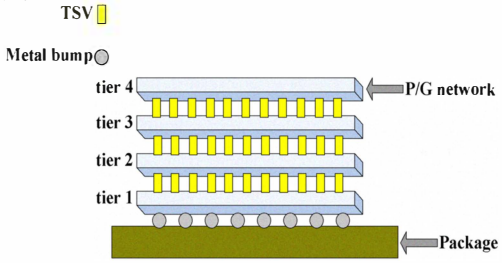

Fig. 2 Top view of the simulation platform

A. Overview of the platform

A 3D P/G network with 4 tiers is illustrated in Fig. 2. Each tier contains a 2D P/G grid and TSVs are used to connect two adjacent tiers together. We assume that Face-to-Back bonding is used in our 3D MPSoC. The vertical interconnect connects the face side of one tier and the back side of the other tier in Face-to-Back bonding. In flip-chip package technology, as Fig. 2 shows, the package I/O pads are connected to the chip I/O pads at the bottommost tier through metal bumps distributed across the chip surface.

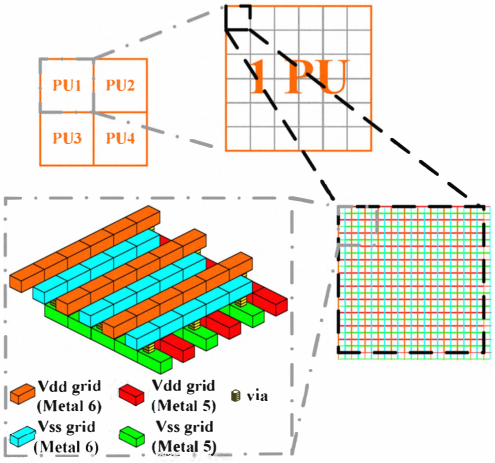

Fig. 3 P/G network architecture of each tier [21]

B. P/G network model

We have design a P/G network for 2D MPSoC in the previous work [21]. The P/G network of each tier in 3D MPSoC is the same as 2D MPSoC. Mesh-based power distribution network is used here.

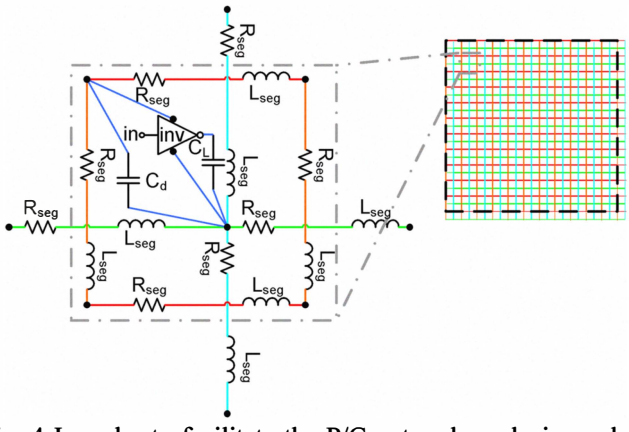

Fig. 4 In order to facilitate the P/G network analysis, each wire segment is modeled as a chain of L-type RLC equivalent circuits. An inverter with a capacitance load is used to imitate the core logic. A decap is connected to the intersection points on the vdd/vss grids [21]

As is shown in Fig. 3, the planar MPSoC chip is

composed of *PU*s organized in 2D-mesh topology. Fig. 4 shows the detailed model of the network. A wire between two adjacent nodes is simply modeled as a lumped resistance R_{seg} and an inductance L_{seg}. C_d represents the capacitance per unit area between a power grid node and the adjacent ground gird node. C_L denotes the load capacitance. We determine the wire segment dimensions and RLC parameters through PTM interconnect model [16]. Both our simulation results and [17] show that on-die inductance has little influence on P/G noise. So the on-chip inductance L_{seg} is neglected during the simulation.

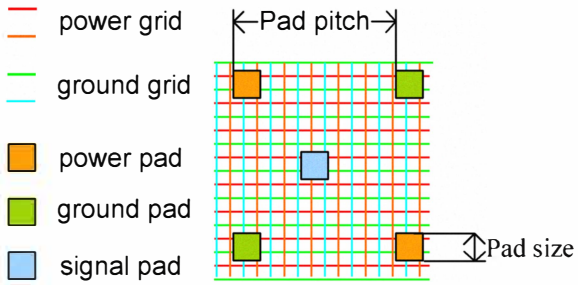

Fig. 5 On-chip power/ground grids and I/O pads on the bottommost die

Inverters are put between power grid and adjacent ground grid node pairs to imitate the *PU* switching activity. We choose the inverter size according to the average power consumption requirement for typical *PU*s. We assume the average power of each *PU* is about 30mW, which is based on ARM11 by scaling down the process parameters. The PTM 45nm bulk CMOS model [16] is used for transistors (Vdd=0.8V). The standard cell library is from the Nangate Open Cell Library [18]. 15% of the total chip area is occupied by decoupling capacitors in the simulation.

C. *Package model*

The flip-chip package has smaller I/O parasitic effect [19] and the distributed pads also help increase total I/O number. Two-thirds of the total pads are used for power distribution [20] in our model. Fig. 5 is a partial picture for P/G pads and grids of the bottommost tier of the 3D MPSoC, which is connected with the package through metal bump.

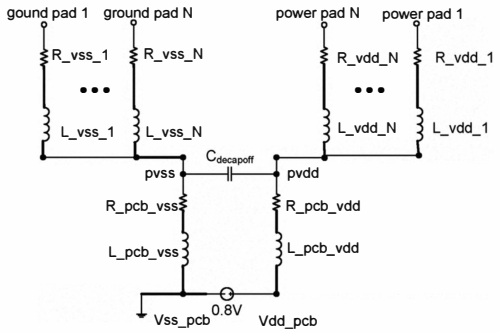

Fig. 6 Package model with package L and off-chip decoupling capacitance

The RLC model of our package model is shown in Fig. 6. The pad and bump are modeled as a package resistance (R_vdd_N and R_vss_N) and a package inductance (L_vdd_N and L_vss_N). The PCB board is modeled as a lumped resistance (R_pcb_vdd/vss) and inductance network (L_pcb_vdd/vss) here. As the power supply is located in the center of the chip in our MPSoC, the values of package resistance and package inductance are in direct proportion to the distance between the current pad and the center pad of the chip. We use this radial network as a simplified package model.

D. *Vertical interconnection model*

When using Face-to-Back bonding, TSVs need to tunnel through the substrate layers of the back side in order to connect that tier. Besides TSV, micro-bumps are also used to connect back-side metal of one tier and the face-side metal of the other one upon it. The circuit model is given in Fig. 7 [22]. Rt and Ct represent the RC of TSV. Cbp1 and Cbp2 denote the capacitance between micro-bump and two substrates of bonded tiers respectively. RCs for the two bonded substrates are modeled as Rsub1 and Csub1, and Rsub2 and Csub2. As the TSV model is capacitance dominant [22], the inductance of TSV and micro-bump is neglected here.

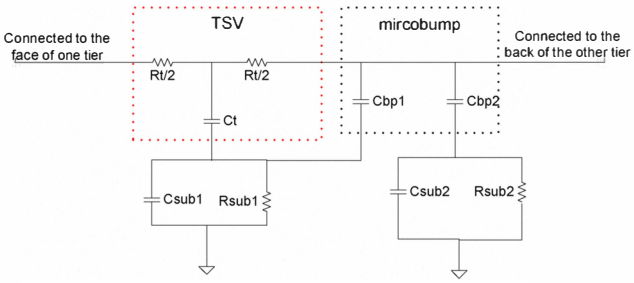

Fig. 7 Vertical interconnection model using Face-to-Back bonding [22]

IV. EXPERIMENTAL RESULTS

We use HSpice for 3D MPSoC P/G noise simulation. The area of a single *PU* is set as a constant 660x660 um2. The clock frequency is 1GHz. Each tier is a 2x2 planar mesh-based MPSoC in following simulations. To explore the impact of TSVs on P/G noise induced by power gating, several experiments are conducted. First different kinds of TSV distributions are explored, including rectangle (case1), cross shape (case2), grid-shape (case3) and uniform distribution (case4), on purpose of finding the proper TSV floorplanning. Secondly, the impact of different number of tiers is explored. Finally, we change the location of active *PU* to observe the voltage deviations. The TSV pitch in the simulation is from 20um to 100um and the side length of TSV pad is 10um [13]. The unit of all the noise values in simulation is mV.

Table I The values of peak noise in each *PU* when PU_{11} is powering on (mV)

	PU_{11}	PU_{12}	PU_{13}	PU_{14}	PU_{21}	PU_{22}	PU_{23}	PU_{24}	PU_{31}	PU_{32}	PU_{33}	PU_{34}	PU_{41}	PU_{42}	PU_{43}	PU_{44}
Case1	186	150	150	142	171	160	160	155	171	160	160	155	171	160	160	155
Case2	195	148	148	142	159	153	153	147	159	153	153	147	159	153	153	147
Case3	191	156	156	149	172	160	160	154	172	160	160	154	172	160	160	154
Case4	185	160	160	154	178	161	162	155	178	162	162	155	178	162	162	156

Table II The values of peak noise in each *PU* of 2D 4x4 MPSoC

D	0	1	$\sqrt{2}$	2	$\sqrt{5}$	$\sqrt{8}$	3	$\sqrt{10}$	$\sqrt{13}$	$\sqrt{18}$
N (mV)	243	149	112	106	97	91	97	93	90	89

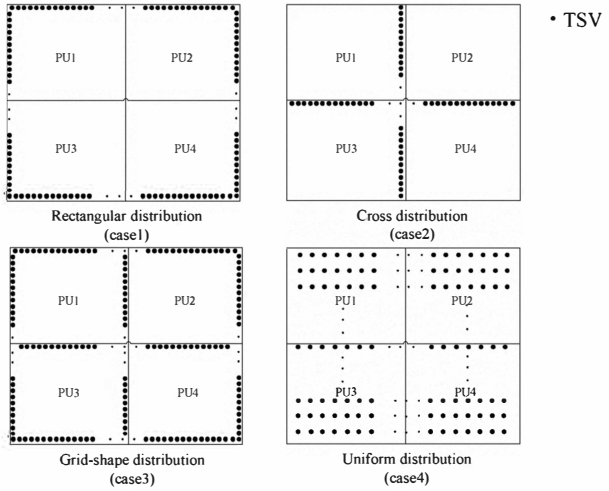

Fig. 8 Different TSV distributions for one layer

A. TSV distributions

Fig. 8 shows four kinds of TSV distributions are explored here. There are four tiers stacked together here. "*PU*1" of different tiers are stacked in the same vertical line.

Table I is values of each peak noise when *PU*1 in the bottommost tier is powering on and all the others are already discharged. PU_{ij} in table I represents *PUj* on tier *i*, where both *i* and *j* are positive integers. The bottommost tier is set to be tier1. The one just upon tier1 is tier2, etc. According to the simulation results, the cross distribution can achieve about a 10mv reduction of P/G noise compared with uniform distribution. The grid-shape distribution and rectangular distribution have the equivalent P/G noise on average. Besides, because the former three distributions (case1, case2 and case3) may introduce cracks during back-grinding and slicing and the noise reduction of cross distribution is not so much more than uniform distribution, actually we tend to choose uniform shape as the P/G TSV distribution.

Table II is the values of peak noise in each *PU* when *PU*s are placed in a 2D mesh-based MPSoC. There are 16*PU*s in the 2D MPSoC in the simulation. In table II, D represents distance from the active *PU* to the other *PU*s. And the side length of a single *PU* is set to be 1. *N* represents peak noise of *PU*s in the special region. The P/G noise in 3D MPSoC is much larger than that in 2D MPSoC. That's because the P/G noise attenuates a little when propagates from one *PU* to another due to shorter interconnections. Hence, noise-related challenges will be much tougher in 3D MPSoC.

B. P/G noise with different number of tiers

In this subsection, we change the total number of tiers from 2 to 6 to explore the P/G noise for different tier numbers. P/G TSVs in each tier are distributed in uniform shape, which is shown in Fig. 8. The active *PU* is *PU*1 in the bottommost tier (tier1).

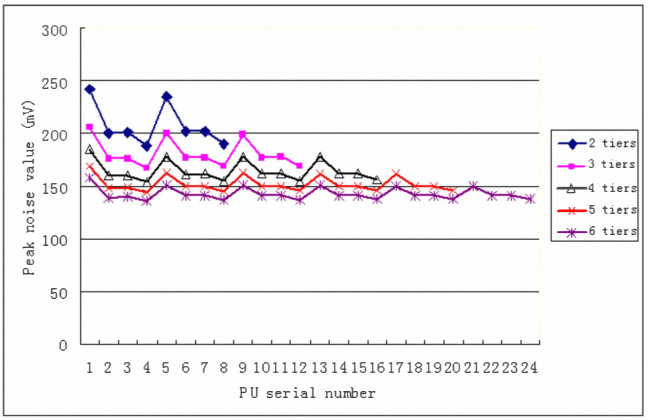

Fig. 9 Simulation results for different number of tiers (the serial number of *PUi* in tier*j* is *i*+(*j*-1)x4)

Fig. 9 shows the simulation results. The *PU* serial number is determined as: the serial number of *PUi* in tier*j* is *i*+(*j*-1)x4. The bottommost tier is set to be tier1. The one just upon tier1 is tier2, etc.

According to Fig. 9, when the *PU* number increases, values of peak noise in each *PU* decrease. Besides, no matter how many tiers there are, all the *PU*s in the same vertical line (ie. *PU*1, *PU*5, *PU*9 and *PU*13 for 4 tiers) have nearly the same P/G noise value. The P/G noise attenuates little in the vertical direction. The parasitic effect of P/G

TSVs is very small and has little impact on P/G noise. So the P/G noise induced by power gating can propagate to other *PU*s nearly without attenuation in the vertical direction, which makes 3D MPSoC more sensitive to P/G noise.

C. P/G noise when different PUs are active

We also choose cross shape as the P/G TSV distribution here. The tier number is set as 4.

The simulation results are shown in Fig. 10. The peak noise value of the active *PU* can achieve about a 5mV reduction when the active *PU* is located in the bottommost tier (*PU*1 is active). The peak noise values of the inactive *PU*s are almost the same no matter where the active *PU* is located. This phenomenon can help designers place *PU*s in 3D MPSoC properly when considering power gating. For *PU*s that are frequently powering on/off, when placed in the bottommost tier, they will have a relatively low P/G noise.

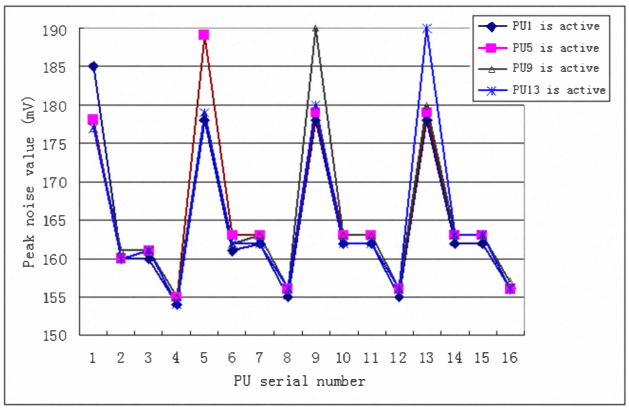

Fig. 10 Simulation results when different *PU*s are active (the serial number of *PUi* in tier*j* is *i*+(*j*-1)x4)

V. CONCLUSIONS AND FUTURE WORK

In this paper, we build a 3D MPSoC P/G noise simulation platform. Then with this platform, we analyze the effect of several key parameters on P/G noise, such as the TSV distribution, tier number and the location of powering on *PU*s. The simulation results show that the cross P/G TSV distribution has the best performance in reducing the P/G noise than the other three cases. The P/G noise attenuates little in the vertical direction in 3D MPSoC. So 3D MPSoC is more sensitive to P/G noise. Besides, the peak noise value of the active *PU* is lower when the active *PU* is located in the bottommost tier, which is useful for 3D MPSoC designers to place *PU*s' allocation when considering power gating. For future work, we will explore the decoupling capacitance in 3D MPSoC.

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